In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A dual-bit split gate flash memory comprising:

a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layers; and

source and drain regions within said substrate and shared by adjacent said memory cells.

2. (Original) The memory according to Claim 1 wherein a channel length under said select gate and said first and second floating gates in between about 0.05 and 0.07 microns in 0.18 micron technology.

3. (Original) The memory according to Claim 1 wherein said select gate comprises:

a polysilicon layer having a thickness of between about 1000 and 1200 Angstroms; and

a dielectric capping layer having a thickness of between about 800 and 1000 Angstroms.

4. (Original) The memory according to Claim 3 wherein said dielectric capping layer comprises high temperature oxide.

5. (Original) The memory according to Claim 1 wherein said select gate oxide has a thickness of between about 29 and 35 Angstroms.

6. (Original) The memory according to Claim 1 wherein said oxide spacer comprises high temperature oxide and has a width of between about 400 and 500 Angstroms.

7. (Original) The memory according to Claim 1 wherein first and second floating gates are isolated from said substrate by a tunneling oxide having a thickness of between about 80 and 100 Angstroms.

8. (Original) The memory according to Claim 1 wherein said first and second floating gates have a thickness of between about 1300 and 1600 Angstroms and a length of between about 500 and 700 Angstroms.

9. (Original) The memory according to Claim 1 wherein said control gate comprises polysilicon having a thickness of between about 2000 and 2400 Angstroms.

10. (Original) The memory according to Claim 1 wherein said dielectric layer comprises a first layer of high temperature oxide, a second layer of silicon nitride, and a third layer of high temperature oxide, each layer having a thickness of between about 60 and 70 Angstroms.

11. - 25. (Canceled)